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A CMOS Vector-Sum Phase Shifter for 5G mm-Wave Application

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Abstract

This paper presents a wideband CMOS vector-sum phase shifter (VSPS) targeting the n260 band of 5G communication. A differential quadrature generator is implemented using a Marchand balun and two 90° coupled-line couplers to improve robustness to process and temperature variations. The quadrature vector signals are combined by a following vector modulator that adopts a double Gilbert-cell topology. The linearity and input-matching performance are enhanced at the expense of extra DC consumption by stacking a current source with high bias. The measurement shows that the VSPS provides a continuous 360° phase shift with an average insertion loss of 16.3 dB at 37 GHz. The root-mean-square (RMS) amplitude and phase errors maintain less than 1.5 dB and 4.9°, respectively, from 30.9 GHz to 41.7 GHz. The input-referred 1-dB compression point is 5.7 dBm at 38 GHz. It is also demonstrated by 484-state measurement that the phase and amplitude can be adjusted in a fine resolution.

Key Words: CMOS, Millimeter-Wave (mm-wave), Phased Array, Vector-Sum Phase Shifter (VSPS), 5G.

I. Introduction

Recently, the millimeter-wave (mm-wave) frequency band has been actively utilized for various applications including 5G communication. To overcome the high channel loss and tight link budget at the mm-wave frequencies, phased arrays have been widely adopted. A phase shifter is an essential circuit block that controls the phase of each channel of the phased-array system.

Several phase shifters with various topologies have been reported for the mm-wave 5G application [1–4]. Nonetheless, there have been few vector-sum phase shifters (VSPS) yet, particularly in the n260 band (37–40 GHz) [1]. The VSPS offers a merit of 360° continuous phase shift with relatively low insertion loss compared to passive-type phase shifters. However, the VSPS would suffer from poor linearity and limited bandwidth. Furthermore, a quadrature generator, e.g., a RC-CR network is required for VSPS and its performance is vulnerable to process and temperature variations of on-chip resistors and capacitors [1].

In this paper, we present a wideband VSPS covering the 5G n260 band. By stacking a current source in the vector modulator with high bias, the linearity and input matching are improved at the expense of DC consumption. The quadrature generator is implemented using a coupled-line coupler, which is relatively robust to process and temperature variations.

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II. VSPS Design

Fig. 1 shows a schematic of the proposed mm-wave VSPS. It consists of a differential quadrature generator and a vector modulator. The differential quadrature generator is implemented using a Marchand balun and two 90° coupled-line couplers. Compared to the RC-CR network, this structure is robust to process and temperature variations. Four quadrature vector signals (V_I^+, V_I^-, V_Q^+, V_Q^-) are generated by feeding each balun output to an individual coupled-line coupler. The balun is implemented with two second top metals (OL) which are edge-coupled to each other. In addition, the 90° coupler is implemented using the top two metals (LB and OL) which are broadside-coupled to each other.

The vector modulator employs two copies of Gilbert cell (M_3–M_8 and M_9–M_{14}). Each Gilbert cell modulates the in-phase vectors (V_I^+ and V_I^-) or the quadrature vectors (V_Q^+ and V_Q^-). By controlling the gate bias of cascode transistors ($V_{c,I}^+$, $V_{c,I}^-$, $V_{c,Q}^+$, $V_{c,Q}^-$), the amplitudes of the in-phase and quadrature signal vectors are changed individually. The differential outputs of the two Gilbert cells are combined in a current domain, thus resulting in a desired phase shift.

The input and output of the VSPS are matched to 50 Ω with transmission lines (TL_1–TL_4 and TL_5–TL_8) and capacitors (C_3–C_4 and C_{13}–C_{14}). One of the differential outputs is terminated by an on-chip 50-Ω resistor for the convenience of measurement. A current source (M_1 and M_2) is connected to each Gilbert cell, which sets a constant bias current. This allows for uniform input matching performance regardless of the phase-shift states. Furthermore, the resulting high bias enhances the linearity at the expense of additional DC consumption.

III. Measurement Results

The mm-wave phase shifter is fabricated in 65-nm CMOS technology. The chip micrograph is shown in the inset of Fig. 1. The chip area is 1.61 × 1.37 mm² including all probing pads.

The measured and simulated phase shift with 4-bit resolution is shown in Fig. 2(a). It can be seen that 16 phase states achieve a full 360° shift with 22.5° separation from 30 to 42 GHz. Fig. 2(b) presents the simulated and measured insertion loss of the

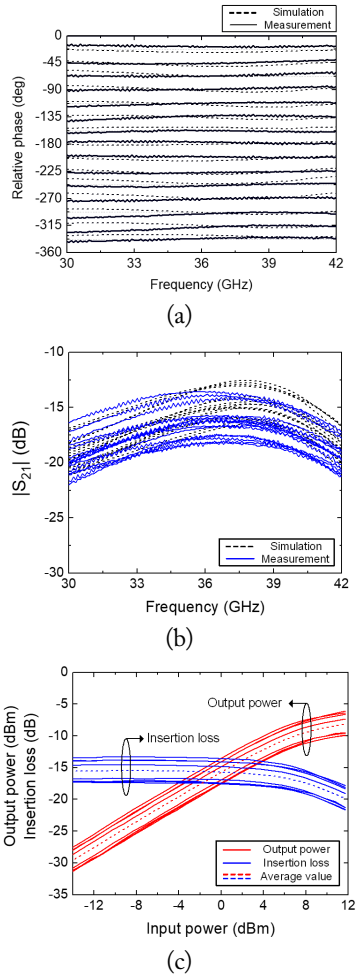

Fig. 2. Measured (a) phase shift with 4-bit resolution, (b) insertion loss of 16 phase states, and (c) output power and insertion loss versus input power at 38 GHz.

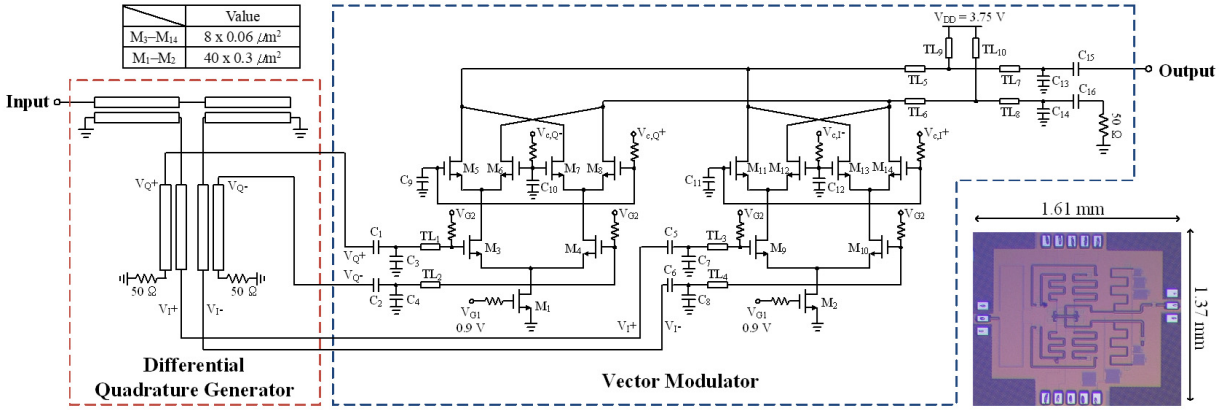

Fig. 1. Schematic and chip photograph of the mm-wave VSPS.

16 phase states. The average loss is 16.3 dB at 37 GHz. The 3-dB bandwidth is 10.8 GHz (30.9–41.7 GHz). It should be noted that the measurement is carried out under a single-ended output condition. Therefore, the insertion loss would be improved by 3 dB in principle if measured differentially. Fig. 2(c) shows the measured output power and insertion loss versus input power at 38 GHz. The average value of input-referred 1-dB compression power is 5.7 dBm at 38 GHz.

Fig. 3(a) shows the root-mean-square (RMS) amplitude and phase errors of the VSPS. With 4-bit resolution, the RMS amplitude and phase errors are 1.3 dB and 1°, respectively, at 38 GHz. The RMS errors maintain less than 1.5 dB and 4.9° from 30.9 to 41.7 GHz. The input and output port matching performance are shown in Fig. 3(b). The input and output ports are well matched over the operating frequency.

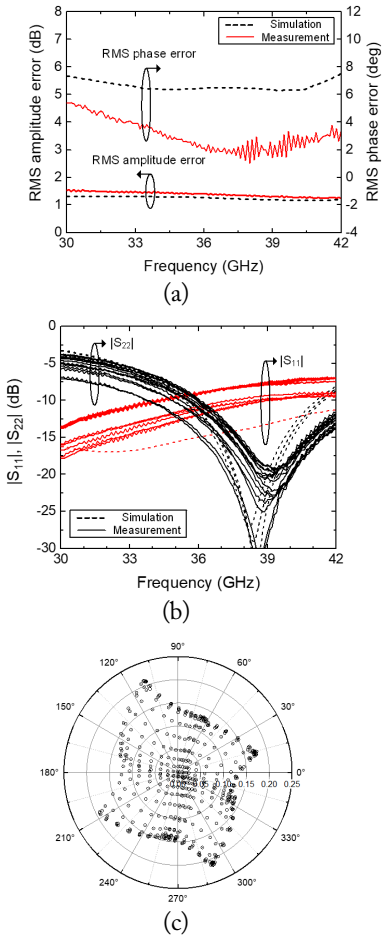

Fig. 3. Measured (a) RMS amplitude and phase errors, (b) input and output matching of 16 phase states, and (c) polar plot of S_{21} for 484 phase states at 38 GHz.

Fig. 3(c) shows a polar plot of the measured S_{21} for 484 phase states. Each of the control voltages ($V_{c,I}^{+}$, $V_{c,I}^{-}$, $V_{c,Q}^{+}$, $V_{c,Q}^{-}$) is individually swept from 2.25 to 3.25 V by 0.1-V step at 38 GHz. It is noted that both the phase and amplitude can be precisely adjusted by fine tuning of the control voltages. This is a significant merit of VSPS over other phase-shifter topologies that can adjust only the phase. The DC power consumption is 45 mW at a supply voltage of 3.75 V.

In Table 1, the proposed VSPS is compared with other published phase shifters in the 5G frequency bands. The VSPS in this work achieves a wide bandwidth with comparable insertion loss and RMS amplitude and phase error. Compared to [2–4], the proposed VSPS provides continuous phase shift and can adjust both amplitude and phase. Compared to previous VSPS [1], this work achieves a wider bandwidth and higher linearity at the cost of DC power consumption.

IV. Conclusion

An mm-wave VSPS for 5G application is implemented in 65-nm CMOS technology. The VSPS exhibits a continuous 360° phase shift with an average insertion loss of 16.3 dB at 37 GHz with a 3-dB bandwidth of 10.8 GHz. Compared to other VSPS in the 5G n260 band, this work achieves a wide bandwidth and high linearity. It is also demonstrated from 484 phase-state measurement that both the phase and amplitude can be adjusted in a fine resolution which is determined by the resolution of control voltage. The proposed VSPS can be adopted in various mm-wave applications including the 5G communication systems.

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Table 1. Performance comparison with previously reported phase shifters for the mm-wave 5G application

Ref.	Tech.	Freq. (GHz)	Resolution	Avg. loss (dB)	RMS amp., phase error	Input P_{1dB} (dBm)	P_{dc} (mW)
Chen et al. [2]	90-nm CMOS	36–40	4 bit	20.2–21	< 2.6 dB, < 2.6°	-	0
Li et al. [3]	65-nm CMOS	32–40	7 bit	16.9–18.1	< 0.38 dB, < 1.6°	-	0
Tsai et al. [4]	65-nm CMOS	27–42	5 bit	12.4 ± 1.2[a]	< 2.1 dB, < 3.8°	7.5[b] @ 39 GHz	0
Xiong et al. [1]	90-nm CMOS	35–41	Cont.	5.9–7	< 0.35 dB, < 5.1°	−2.8[b] @ 35.5 GHz	17.6
This work	65-nm CMOS	30.9–41.7	Cont.	16.3–19.3	< 1.5 dB, < 4.9°	5.7	45

P_{1dB} = power at the 1-dB compression point.

[a] Measured insertion loss at 39 GHz.

[b] Read from a plot of the article.

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